REMARKS

The Examiner's Action mailed on January 22, 2009, has been received and its contents carefully considered.

In this Amendment, Applicant has amended claims 6 and 7, and added claims 8-13. Claims 6 and 7 are the independent claims, and claims 6-13 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has rejected claim 6 as being anticipated by *Kumar et al.* (US 6,573,534) (hereafter simply *Kumar*). Claim 6 is not anticipated by the cited reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 U.S.C. § 102 only if all the features and all the relationships recited in the claim are taught by the referenced structure either by clear disclosure or under the principle of inherency.

Claim 6 is directed to a semiconductor device that has an epitaxial layer, an impurity region, a further impurity region and a channel region. The epitaxial layer has a first conductivity. The impurity region is formed by doping a surface portion of the epitaxial layer with an impurity of a second conductivity. The impurity region has a profile such that a near surface thereof has a relatively low second-conductivity impurity concentration and a deep portion thereof has a relatively high second-conductivity impurity concentration. A second-conductivity impurity concentration in an outermost surface portion of the impurity region is controlled to be lower than a first-conductivity impurity concentration in the epitaxial layer. The further impurity region doped with an impurity of the first conductivity is formed on a surface portion of the impurity region.

Claim 6 further recites that the channel region having the first conductivity is formed in the outmost surface portion between the epitaxial layer and the further impurity region of the first conductivity.

Claim 6 has been amended to recite that an impurity concentration of the first conductivity in the channel region is lower than the second-conductivity impurity concentration in the deep portion of the impurity region of the second conductivity, which is supported by the following paragraphs of the specification and Figures 1-6.

[0024] Where a p-type impurity concentration in an outermost surface portion of the p-type impurity region 3 is lower than the n-type impurity concentration of the n^--type SiC semiconductor epitaxial layer 2(e.g., $10^{16}/cm^3$), an accumulation MOSFET structure can be provided in which an n^--type conductivity appears, as shown in Fig. 3, in the surface portion (channel region) of the p-type impurity region 3 and the n^--type channel region serves as an accumulation layer 31. Therefore, the carrier mobility in the channel is further improved.

[0031] Since the n-type impurity concentration (atom density) in the n^--type SiC semiconductor epitaxial layer 12 is generally constant on the order of $10^{16}/cm^3$, the p-type impurity concentration in the surface portion (channel region) of the p-type impurity region 13 is lower than the n-type impurity concentration. As a result, an n-type conductivity appears in the surface portion of the p-type impurity region 13 to form the n-type accumulation layer 16.

[0032] As shown in Fig. 6, the accumulation MOSFET with its n-type accumulation layer 16 thus formed has more excellent characteristics than a prior-art MOSFET having a p-type impurity region formed as having substantially the same depth as the p-type impurity region 13 in a surface portion of an n^--type SiC semiconductor epitaxial layer by performing ion implantation with four different levels of implantation energy (four-step ion implantation).

[0034] A formation of a buried channel such as the n-type accumulation layer 16 may be achieved by forming an n-type layer by epitaxial growth after the formation of the p-type impurity region (e.g., Japanese Unexamined Patent Publication No. 10-308510). Alternatively, the formation may be achieved by performing multi-step ion implantation to selectively implant the n-type impurity into the p-type impurity region after the formation of the p-type impurity region (e.g., Japanese Unexamined Patent Publication No. 11-261061).

[0035] Where the buried channel is formed by the epitaxial growth, the epitaxial growth should be stopped at an initial stage to provide a thin n-type layer having a depth of about 0.1 to 0.2μm. However, it is difficult to precisely control an impurity concentration and a depth at the initial stage of the epitaxial growth. Therefore, it is impossible to control the impurity concentration and the depth of the buried channel as designed, which presents a problem that an accumulation MOSFET is liable to be of a normally ON type.

[0036] In the ion implantation, it is possible to precisely control the depth of the buried channel. However, the n-type impurity is implanted with a high concentration to cancel the p-type conductivity of the p-type impurity region, so that the buried channel has a high impurity concentration. This results in a problem that the impurity concentration of the buried channel cannot be controlled as designed, because a rate of impurity activation by annealing after the ion implantation is unstable. The buried channel having a high impurity concentration also suffers from a problem that carriers are susceptible to coulomb scattering and, hence, carrier mobility in the channel is lower.

[0037] In contrast, the method according to this embodiment (involving the formation of the **n-type accumulation layer 16**) is free from the problem encountered where the buried channel is formed by the epitaxial growth. Further, **the n-type accumulation layer 16 has a low impurity concentration**, so that the accumulation MOSFET is manufactured as having a normally OFF characteristic as designed without an influence of a rate of the activation by the annealing. Further, the n-type accumulation layer 16 has a high carrier mobility with a smaller degree of coulomb scattering of the carriers.

The Examiner equates the layer 5b disclosed by *Kumar* with the channel region recited in claim 6, and equates the layer 5a disclosed by *Kumar* with the further impurity region recited in claim 6. (see the Examiner's Action, page 3, lines 3-7). The Examiner also equates p+layer 30a and 30b disclosed by *Kumar* with the deep portion recited in claim 6. (see the Action, page 2, lines 4-5 from the bottom).

However, in *Kumar*, there is no disclosure that the impurity concentration of the n+ conductivity in the layer 5b (equated with channel region by the Examiner) is lower than the impurity concentration of the p+ conductivity in the layers 30a and 30b (equated with deep portion by the Examiner), as would be required by amended claim 6. *Kumar* does not disclosure any relation between the p-conductivity concentration of a deep portion of the p-layer 3a and an n-conductivity concentration of the n-layer 5b.

It is thus submitted that claim 6 is *prima facie* patentably distinguishable over the cited reference. It is requested that this claim be allowed, and the rejection be withdrawn.

The Examiner has further rejected claim 7 as being obvious over *Kumar* in view of *Huang* (USP 6,373,102), and further in view of *Pavlidis et al.* (USP 4,827,319).

Claim 7 recites as follows:

doping a surface portion of the silicon carbide semiconductor epitaxial layer with an impurity of a second conductivity to form **an impurity region** having a profile such that **a near surface** thereof has a relatively low second-conductivity impurity concentration and **a deep portion** thereof has a relatively high second-conductivity impurity concentration,

wherein the surface portion of the silicon carbide semiconductor epitaxial layer is doped with the impurity of the second conductivity **by single-step ion implantation** in the impurity region forming step, the single-step ion implantation being performed with a single constant level of implantation energy,

wherein a first-conductivity impurity concentration in the epitaxial layer is higher than a second-conductivity impurity concentration in an outermost surface portion of the impurity region, so as to form **a channel region** having the first conductivity in the outermost surface portion of the impurity region

Thus, in claim 7, the entire impurity region and the channel region are formed by the single-step ion implantation. Accordingly, both the deep portion and the near surface of the impurity region are formed by the same single-step ion implantation.

The Examiner equates the layer 3a (Fig. disclosed by *Kumar* with the claimed near surface, and equates the layer 30a disclosed by *Kumar* with the claimed deep portion. However, the layer 30a and the layer 3a are not formed by the same single-step ion implantation. The layer 3a is formed by an ion implantation shown in Figure 34, and then the layer 30a is formed by another separate ion implantation shown in Figure 38.

Moreover, because the layer 30a is formed on sections not overlapping the source region (see *Kumar*, col. 19, lines 48-50), the insulating film 22 is used as a mask for B+ ion implantation to form deep base layers 30a, 30b (see *Kumar*, col. 21, lines 1-18 and Figure 38). Thus, the layer 3a directly under the source region cannot be formed by the same ion implantation by which the layer 30a is formed.

Further, the claimed channel region is also formed by the same single-step ion implantation. In contrast, *Kumar*'s channel regions 5a or 5b are formed by an implantation (as shown in *Kumar*'s Figure 35) that is different from another implantation for forming the layer 3a (as shown in *Kumar*'s Figure 35).

In addition, claim 7 has been amended to further recite that an impurity concentration of the first conductivity in the channel region is lower than the second-conductivity impurity concentration in the deep portion of the impurity region. As noted above, the deep portion should be a portion formed by the single ion implantation.

The Examiner equates the ion implantation shown in *Kumar*'s Figures 33 and 34 with the claimed single-step ion implantation (see the Action, page 4, last line, through page 5, line 9). Only the layer 3a is formed by the ion implantation shown in Figure 33 and 34. Thus, the layer 3a, rather than the layer 30a, may be equated with the claimed impurity region. And, a deep portion of the layer 3a may be equated with the claimed deep portion of the impurity region.

However, in *Kumar*, there is no disclosure or suggestion about any relation between the p-conductivity concentration of a deep portion of the p-layer 3a and an n-conductivity concentration of the n-layer 5a. In other words, *Kumar* does not disclose or suggest that the impurity concentration of the n+ conductivity in the layer 5a is lower than the p- impurity concentration in a deep portion of the layer 3a, as would be required by amended claim 7.

Because neither *Huang* nor *Pavlidis et al.* overcome the above-noted deficiencies of *Kumar*, it is submitted that claim 7 is *prima facie* patentably distinguishable over the cited references. It is requested that this claim be allowed, and the rejection be withdrawn.

Claims 8-13 have been newly added. Because claims 8-13 depend respectively from independent claims 6 and 7, it is submitted that claims 8-13 are *prima facie* patentably distinguishable over the cited references for at least the same reasons as claim 6 and 7.

In addition, claim 8 further recites that, as exemplary illustrated in Applicant's Figure 1, the further impurity region 4 is spaced apart from peripheral edges of the impurity region 3 of the second conductivity, such that side surfaces of the further impurity region 4 come in contact with and are covered with the impurity region 3 of the second conductivity. In contrast, as shown in *Kumar*'s Figure 41, peripheral edge of the layer 5a (equated by the Examiner with the claimed further impurity region) is linearly connected with the peripheral edge of the layer 3a. Thus, the layer 5a is not spaced apart from the peripheral edge of the layer 3a. Moreover, the side surfaces of the layer 5a do not come in contact with or are covered with the layer 3a, as would be required by claim 8. Rather, the right and left side surfaces of the layer 5a come in contact with and are covered with the layer 5b and the layer 4a respectively. (see Figure 41).

Claim 9 further recites that, as exemplary shown in Figure 3, the channel region 31 is disposed between the epitaxial layer 2 and the further impurity region 4 of the first conductivity, such that one side surface (e.g., left side surface) of the channel region 31 comes in contact with the epitaxial layer 2 and the other side surface (e.g., right side surface) of the channel region 31 comes in contact with the further impurity region 4 of the first conductivity. In contrast, as shown in *Kumar*'s Figure 41, both side surfaces of *Kumar*'s layer 5b come in contact with the layer 5a.

Claims 10 and 13 further recite that, as shown in Figures 1 and 3, the deep portion the impurity region 3 includes a portion that is disposed directly under the further

impurity region 4. In contrast, *Kumar*'s layer 30a is not disposed directly under the layer 5a or the layer 4a.

Claim 11 further recites that the first-conductivity impurity concentration in the silicon carbide semiconductor epitaxial layer is **constant** (see the specification, page 15, line 3), and the constant first-conductivity impurity concentration in the epitaxial layer is higher than the second-conductivity impurity concentration in an outermost surface portion of the impurity region. In contrast, in *Kumar,* the concentration in the layer 5b is different from the concentration in layer 2. Thus, *Kumar's* layer 5b (whose concentration differs from that of the layer 2) cannot be equivalent to the claimed epitaxial layer.

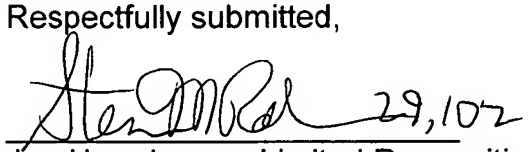
Claim 12 further recites a step of doping a surface portion of the impurity region of the second conductivity with an impurity of the first conductivity to form a further impurity region, wherein the further impurity region is spaced apart from peripheral edges of the impurity region of the second conductivity, such that side surfaces of the further impurity region come in contact with and is covered by the impurity region of the second conductivity, which are similarly recited in claims 8 and 9.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fees be required, the Commissioner is hereby authorized to charge such fees to our deposit account No. 18-0002, and is requested to advise us accordingly.

Respectfully submitted,



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